IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): RAJAGOPALAN, Sarathy *et al.*

Serial No.: 09/465,131

Filed: December 16, 1999

For: METHOD AND APPARATUS FOR THERMAL PROFILING OF FLIP-CHIP PACKAGES

Art Unit: 2859

Examiner: Guadalupe, Yaritza

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date below.

March 10, 2004 Rhonda L. Mason

Rhonda L. Mason

RESPONSE TO ORDER RETURNING UNDOCKETED APPEAL

-AND-

AMENDED APPEAL BRIEF UNDER 37 C.F.R. § 1.196(d)

Mail Stop: AFTER FINAL (EXPEDITED PROCEDURE)
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Appellant hereby requests reinstatement of the appeal of the final rejection of Claims 1-6 in the subject application and submits this amended appeal brief (in triplicate) under 37 C.F.R. § 1.196(d) in response to the Order Returning Undocketed Appeal of January 20, 2004 and the telephone message from the examiner of March 5, 2004 requesting that Applicant submit a response to the Order Returning Undocketed Appeal.

(1) Real Party in Interest

The real party in interest in the subject application is LSI Logic Corporation.

(2) Related Appeals and Interferences

No related appeals or interferences are known to appellant.

(3) Status of Claims

Claims 1-6 are pending in the subject application.

Claims 1, 4 and 5 stand finally rejected under 35 U.S.C. § 103(a) as being unpatentable over admitted prior art (APA) in view of U.S. Patent 5,997,174 to Wyland (*Wyland*).

Claims 2 and 3 stand finally rejected under 35 USC §103(a) as being unpatentable over admitted prior art in view of *Wyland* as applied to Claims 1, 4 and 5 and further in view of U.S. Patent No. 6,131,579 to Thorson et al. (*Thorson*).

Claim 6 stands finally rejected under 35 USC §103(a) as being unpatentable over admitted prior art in view of *Wyland* and further in view of U.S. Patent No. 5,585,577 to Lemoine (*Lemoine*).

(4) Status of Amendments

The amendments filed on May 8, 2001 (Amendment "A"), September 6, 2001 (Amendment "B"), October 24, 2001 (Amendment "C"), and May 1, 2002 (Amendment "D") have been entered.

Amendment "E" is submitted herewith to correct the formal errors noted by the Board in the Supplemental Appeal

Brief filed on June 11, 2003.

(5) Summary of Invention

The present invention provides a thermal profiling device for accurately measuring the temperature at the interface between a semiconductor die and a packaging substrate of an integrated circuit during a reflow process in which the die is attached to the substrate. In one aspect of the present invention, a thermal profiling device for a flip-chip integrated circuit includes a packaging substrate of a flip-chip integrated circuit; a semiconductor die of the flip-chip integrated circuit having an active circuit surface for interconnecting the semiconductor die to the packaging substrate wherein the active circuit surface is secured to an upper surface of the packaging substrate; and a thermocouple secured directly to the active circuit surface of the semiconductor die for measuring a temperature of the active circuit surface of the semiconductor die during a reflow process.

(6) Issues on Appeal

The following issues are on appeal:

Issue 1: Whether motivation exists for modifying APA by *Wyland*; and

Issue 2: Whether modifying APA by *Wyland* would arrive at the claimed invention.

(7) Grouping of Claims

A statement that the claims of a group do not stand or fall together is not included with this supplemental appeal brief.

(8) Argument

No motivation exists for modifying APA by *Wyland*

Claim 1 recites a thermocouple secured directly to the active circuit surface of a semiconductor die for measuring a temperature of the active circuit surface of the semiconductor die during a reflow process. The rejection admits that APA does not disclose the thermocouple secured directly to the active circuit surface of the semiconductor die as recited in Claim 1. The rejection argues that *Wyland* discloses locating a thermocouple (117) secured on a junction between surfaces (113, 114) for measuring and controlling a junction/interface temperature and that it would be obvious to modify APA by providing a thermocouple secured to the semiconductor die for measuring the junction/interface temperature as taught by *Wyland* to provide an enhancement for measuring die interface temperature. Appellant traverses the rejection as follows.

The rejection errs in alleging that the method of measuring temperature taught by *Wyland* teaches or suggests providing a thermocouple secured to the semiconductor die. As *Wyland* shows in FIG. 1A and explains in the abstract and column 4, lines 47 *et seq.*, the thermocouple (117) is used to determine the junction temperature of a semiconductor die (122) inside a component package (121) by measuring the

thermal resistivity of a board or coupon (113) outside the component package (121). The thermocouple (117) is attached between the surfaces of the coupon (113) and the thermally conductive substrate (114) outside the component package (121) away from the semiconductor die (122). Because the thermocouple (117) is secured outside the component package (121) away from the semiconductor die (122), *Wyland* teaches away from the claimed invention that recites securing the thermocouple directly to the active circuit surface of a semiconductor die. Because *Wyland* teaches away from the claimed invention, there is no motivation to modify APA by *Wyland* as required by MPEP § 2143 (2100-124,125).

Modifying APA by *Wyland* would fail to arrive at the claimed invention

Even if there were motivation to modify APA by *Wyland*, such a modification would fail to arrive at the claimed invention. As shown in FIG. 1A, *Wyland* teaches securing the thermocouple (117) outside the component package (121) away from the active circuit surface of the semiconductor die (122).

Because modifying APA according to the teaching of *Wyland* would not result in securing the claimed thermocouple directly to the active circuit surface of the semiconductor die as recited in Claims 1 and 6, the combination of APA and *Wyland* fails to arrive at the claimed invention as required by MPEP § 706.02(j) (700-45).

Conclusion

Because no motivation exists for modifying APA according to the teaching of *Wyland*, and because such a

modification would not arrive at the claimed invention, the rejection of Claims 1 and 6 under 35 U.S.C. § 103 over *Wyland* lacks reasonable support. Because the rejection lacks reasonable support, Applicant requests that the rejection be withdrawn.

Because the rejections of Claims 2-5 rely on the same errors made in the rejection of Claims 1 and 6, the rejections of Claims 2-5 under 35 U.S.C. § 103 also lack reasonable support. Because the rejections of Claims 2-5 lack reasonable support, Applicant requests that the rejections of Claims 2-5 be withdrawn.

Respectfully submitted,

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APPENDIX

Claims on Appeal

1. A thermal profiling device for a flip-chip integrated circuit comprising:

a packaging substrate of a flip-chip integrated circuit;

a semiconductor die of the flip-chip integrated circuit having an active circuit surface for interconnecting the semiconductor die to the packaging substrate wherein the active circuit surface is secured directly to an upper surface of the packaging substrate; and

a thermocouple secured directly to the active circuit surface of the semiconductor die for measuring a temperature of the active circuit surface of the semiconductor die during a reflow process.

2. The thermal profiling device of Claim 1 wherein the thermocouple is secured using an adhesive.

3. The thermal profiling device of Claim 2 wherein the adhesive comprises an epoxy.

4. The thermal profiling device of Claim 1 wherein the active circuit surface has electrically conductive bumps formed thereon and the upper surface of the packaging substrate includes a plurality of bonding pads wherein the semiconductor die is positioned on the packaging substrate such that the electrically conductive bumps are in electrical contact with the plurality of bonding pads.

5. The thermal profiling device of Claim 4 wherein the packaging substrate and the semiconductor die are secured

in place by a solder bond between the electrically conductive bumps and the plurality of bonding pads.

6. A thermal profiling device comprising:

a packaging substrate of a flip-chip integrated circuit having a first surface and a second opposite surface;

an opening passing through the second opposite surface and through the first surface of the packaging substrate;

a semiconductor die of the flip-chip integrated circuit having an active circuit surface for interconnecting the semiconductor die to the packaging substrate wherein the active circuit surface is secured directly to the first surface of the packaging substrate; and

a thermocouple secured directly to the active circuit surface of the semiconductor die through the opening for measuring a temperature of the active circuit surface of the semiconductor die during a reflow process.